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10-24-03

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Group Art Unit: 2123
Terry Lee Goode	)	Examiner: Unknown
Appln No. 09/841,974	)	Confirmation No. 6204
Filed: April 24, 2001	)	
For: EMULATOR WITH SWITCHING NETWORK CONNECTIONS	)	Atty. Dkt. No. 003921.00011

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

Sir:

In accordance with 37 C.F.R. §1.97 and §1.98, enclosed is a PTO Form-1449 listing art for consideration by the Examiner. We hereby certify under 37 C.F.R. §1.97(e)(1) that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

We further certify under 37 C.F.R. § 1.704 (d) that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and that this communication was not received by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this Information Disclosure Statement.

These documents were cited by the International Searching Authority (the European Patent Office) for corresponding International Patent Application No.

PCT/US02/12603. The search report was mailed by the ISA on October 2, 2003. A copy of the search report is also enclosed.

Consideration of this information is respectfully requested.

The submission of the listed documents is not intended as an admission that any such documents constitute prior art against the claims of the present application. Applicant does not waive any right to take any action that would be appropriate to antedate or otherwise remove any listed documents as a competent reference against the claims of the present application.

Respectfully submitted,

Dated: October 10, 2003

By: 
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Information Disclosure Statement
Serial No. 09/841,974

Sheet 1 of 1

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. 003921.00011	SERIAL NUMBER 09/841,974
	APPLICANT Terry Lee Goode	
	FILING DATE April 24, 2001	GROUP ART UNIT ~~2123~~ 2128

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

/S.L./	Search Report
/S.L./	D. Bursky, "FPGA Combines Multiple Serial Interfaces And Logic", Electronic Design, pgs. 74-77, October 2, 2000.
/S.L./	Jianmin Li et al., "Routability Improvement Using Dynamic Interconnect Architecture", IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, Vol. 6, No. 3, September 1998, pp. 498-501.
/S.L./	Jonathan Babb et al., "Logic Emulation with Virtual Wires", IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, Vol. 16, No. 6, pgs. 609-626, June 1997.
/S.L./	Joseph Varghese et al., "An Efficient Logic Emulation System", IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, Vol. 1, No. 2, pgs. 171-174, June 1993.

EXAMINER /Suzanne Lo/	DATE CONSIDERED 03/01/2008

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.